

Please amend the specification as follows:

[0001] The present application is a continuation-in-part of U.S. Patent Application No. 09 819,344 (~~Atty. Dkt. No. 39153-406 (F1061)~~) by Okoroanyanwu, et al. entitled "Process for Reducing the Critical Dimensions of Integrated Circuit Device Features" ~~filed March 28, 2001~~; U.S. Patent Application No. 09 819,692 (~~Atty. Dkt. No. 39153-404 (F0943)~~) by Okoroanyanwu et al., entitled "Process for Preventing Deformation of Patterned Photoresist Features;" and U.S. Patent Application No. 09/819,342 (~~Atty. Dkt. No. 39153-403 (F0942)~~) by Okoroanyanwu et al., entitled "Process for Forming Sub-lithographic Photoresist Features by Modification of the Photoresist Surface." The present application is also related to U.S. Patent Application No. 09/820,143 (~~Atty. Dkt. No. 39153-405 (F0945)~~) by Okoroanyanwu et al., entitled "Improving SEM Inspection and Analysis of Patterned Photoresist Features;" U.S. Patent Application No. 09/819,343 (~~Atty. Dkt. No. 39153-298 (F0785)~~) by Gabriel et al., entitled "Selective Photoresist Hardening to Facilitate Lateral Trimming;" and U.S. Patent Application No. 09/819,552 (~~Atty. Dkt. No. 39153-310 (F0797)~~) by Gabriel et al., entitled "Process for Improving the Etch Stability of Ultra-Thin Photoresist." [[, .]] All of the above application were filed on March 28, 2001 and are assigned to the Assignee of the present application.